

FIG. 1

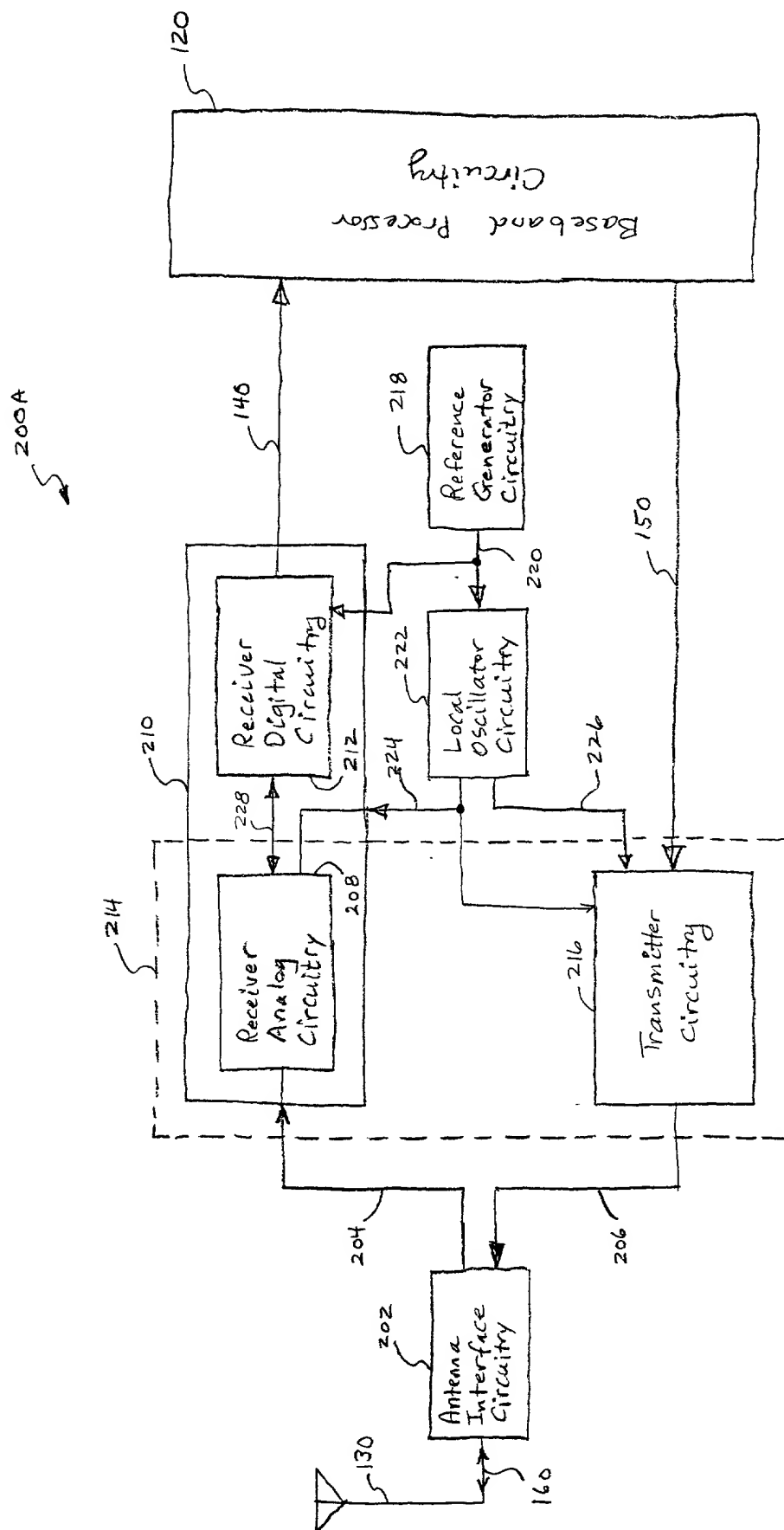


FIG. 2A

200B

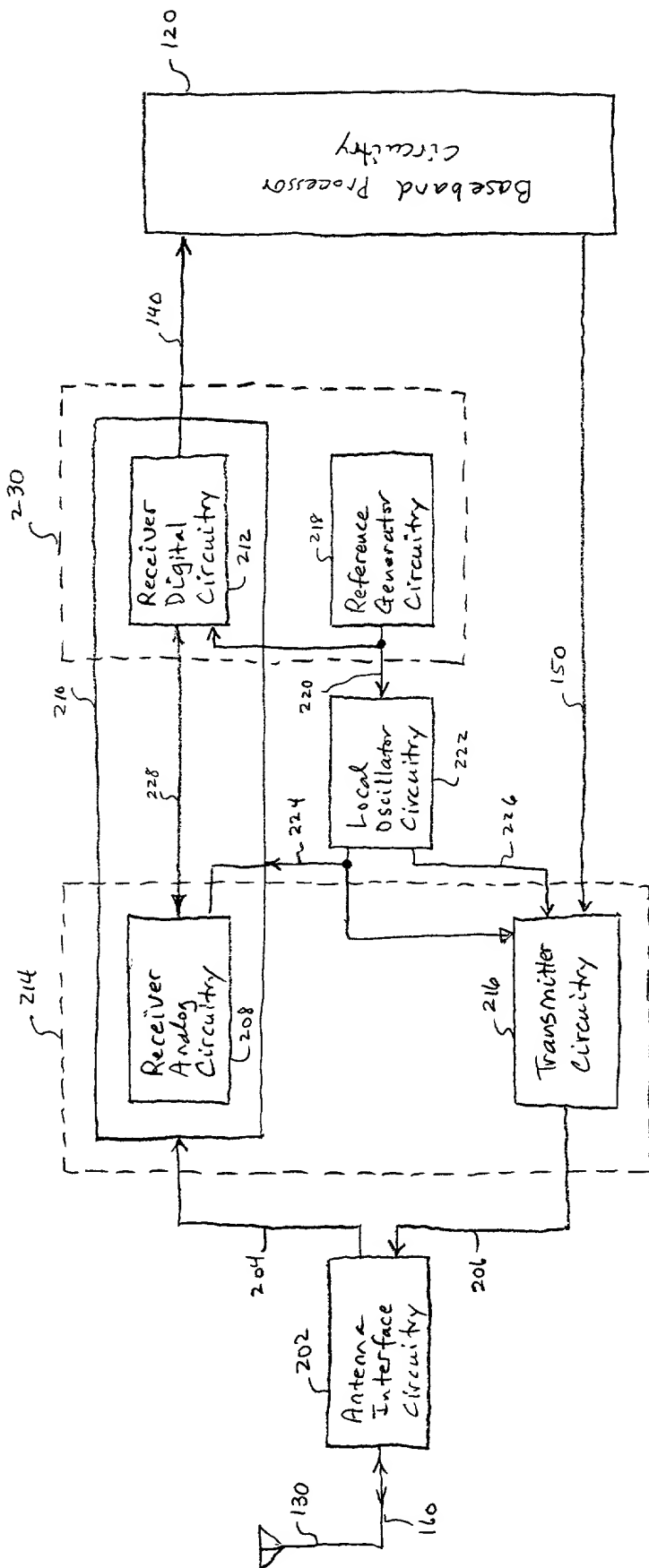


FIG. 2B

FIG. 20C

200C

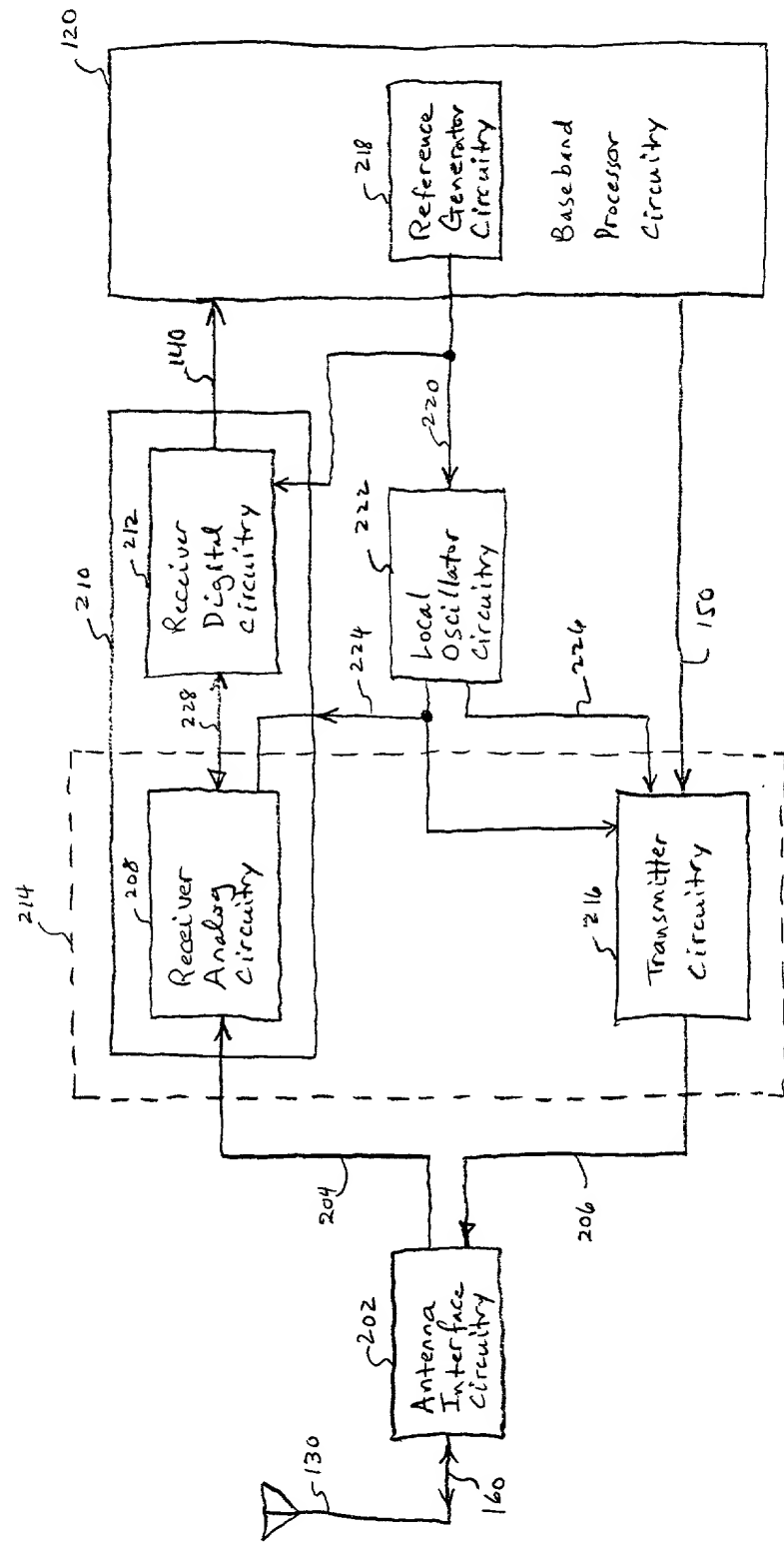


FIG. 20

200D

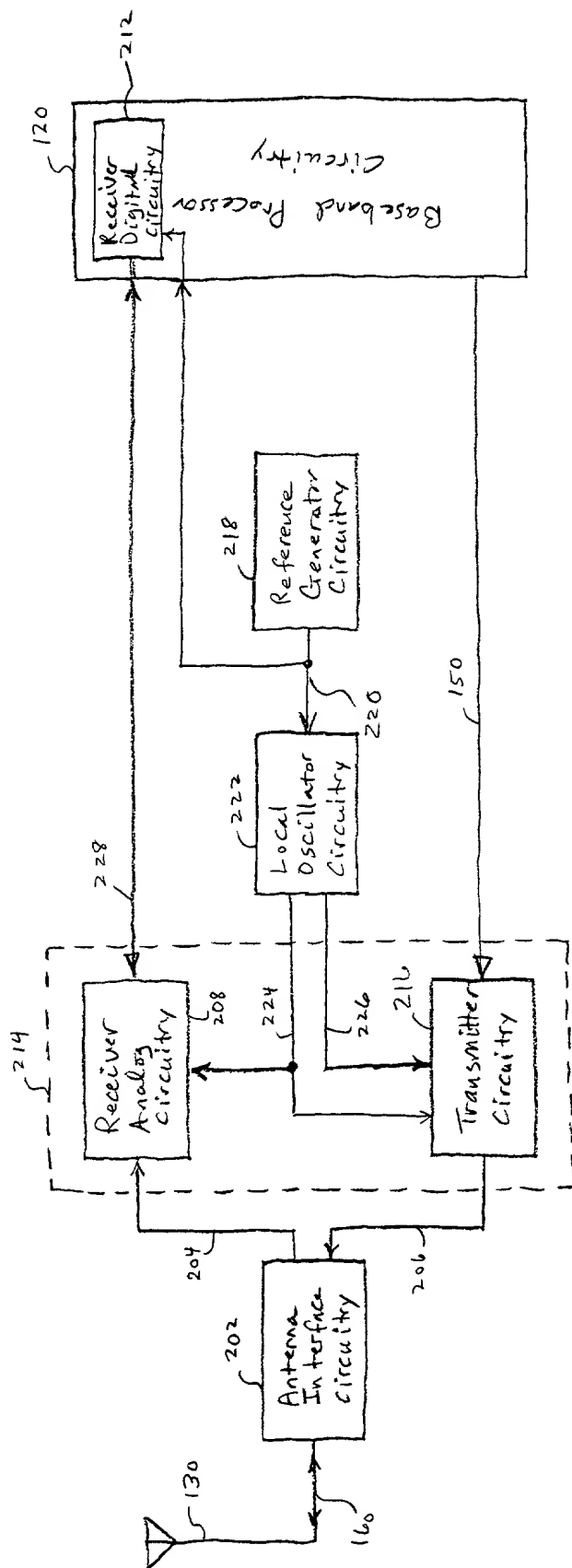


FIG. 2D

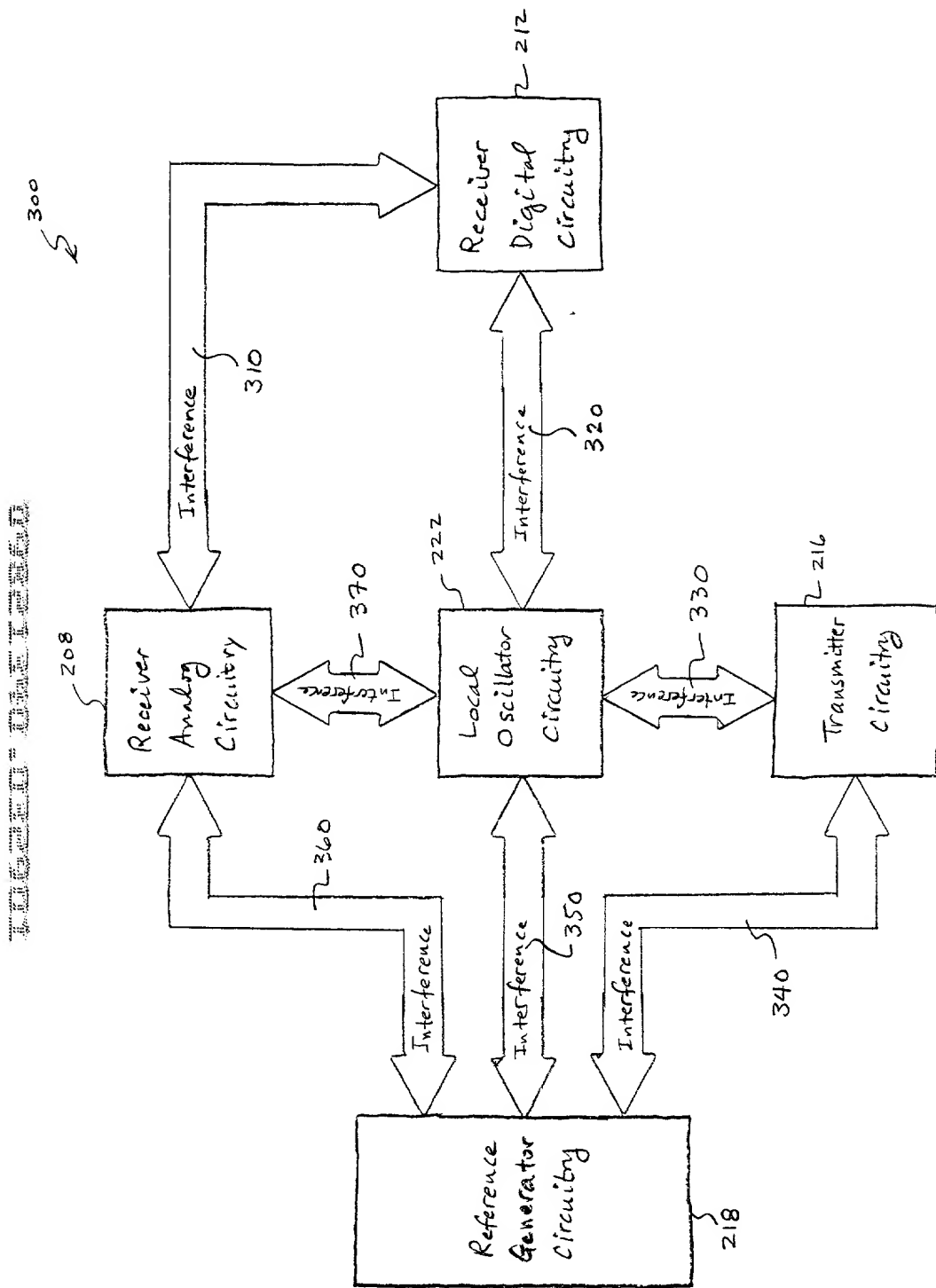


FIG. 3

400

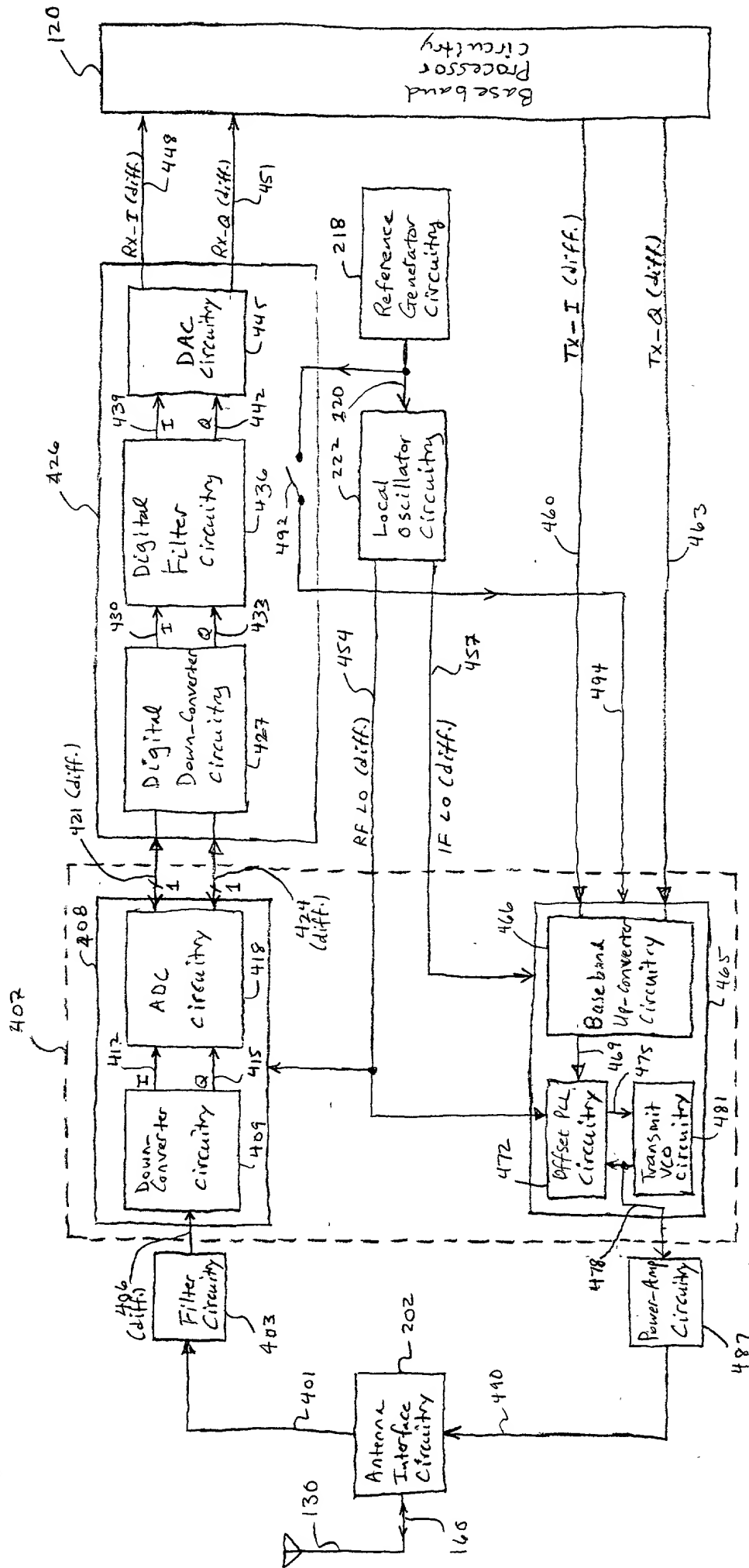


FIG. 4

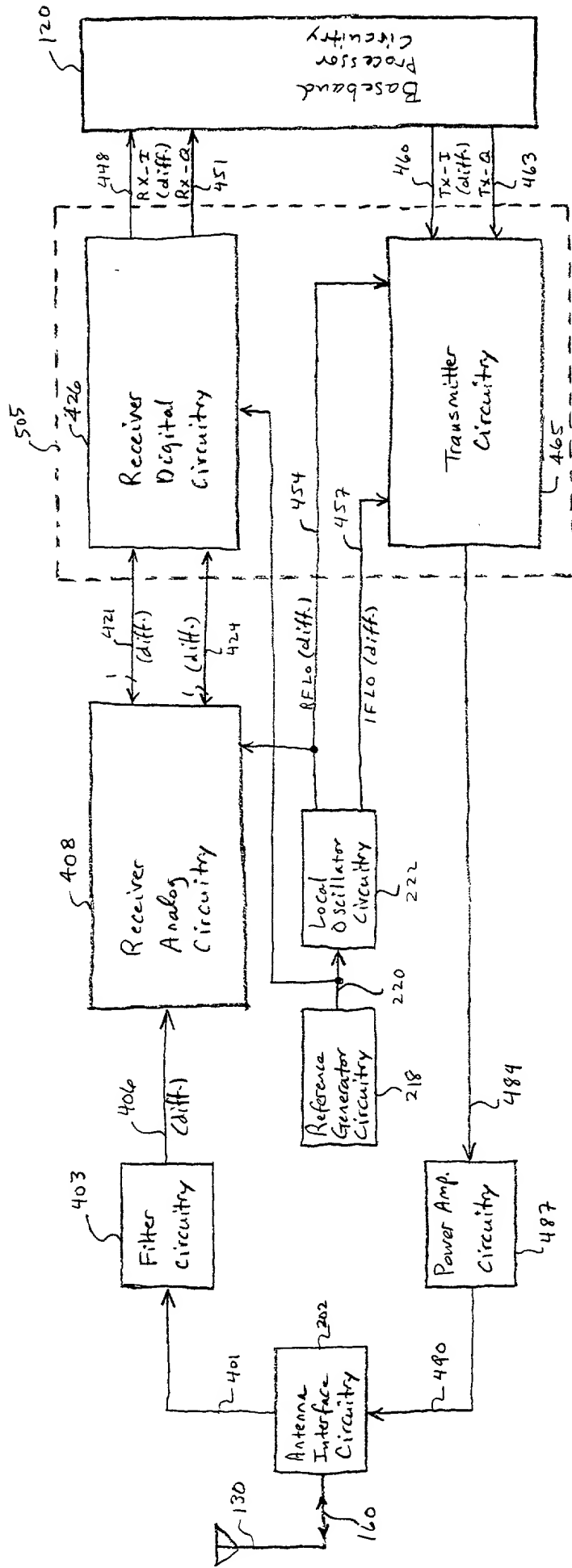


FIG. 5



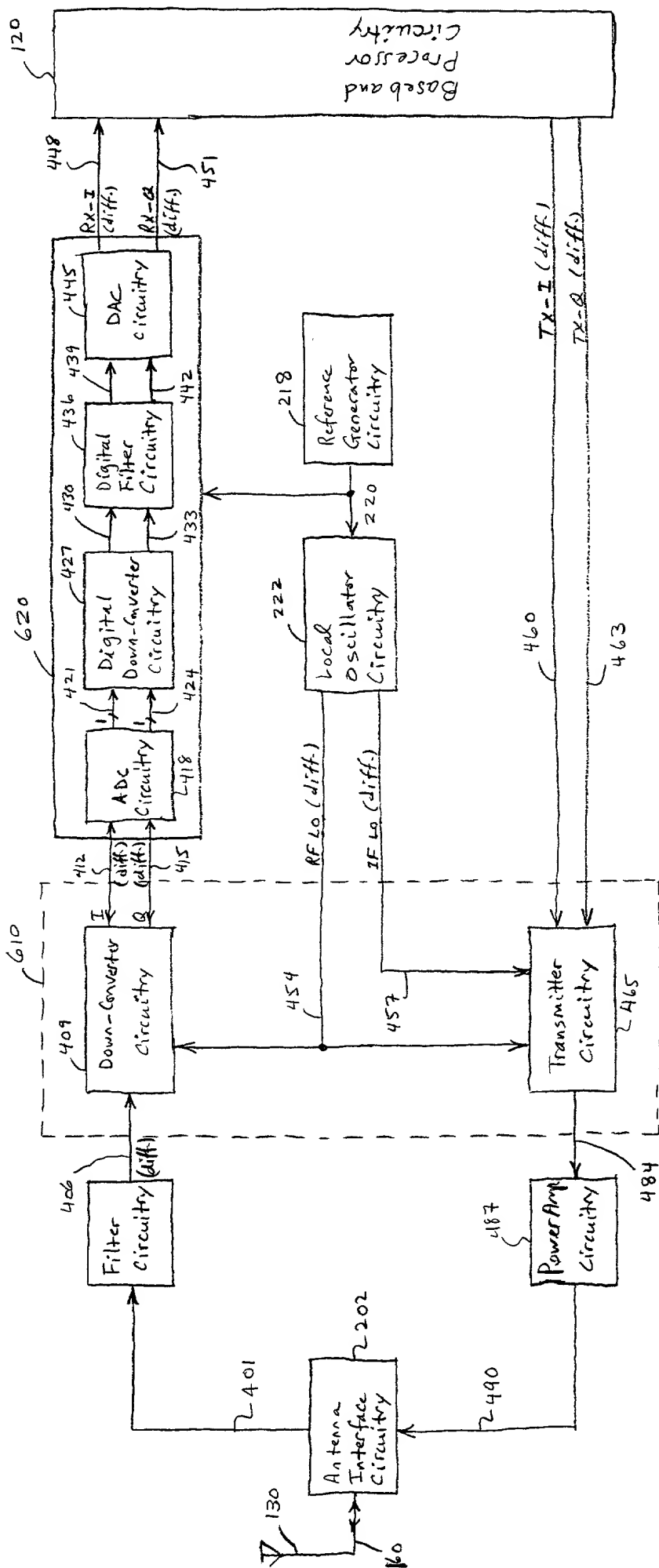


FIG. 6

700

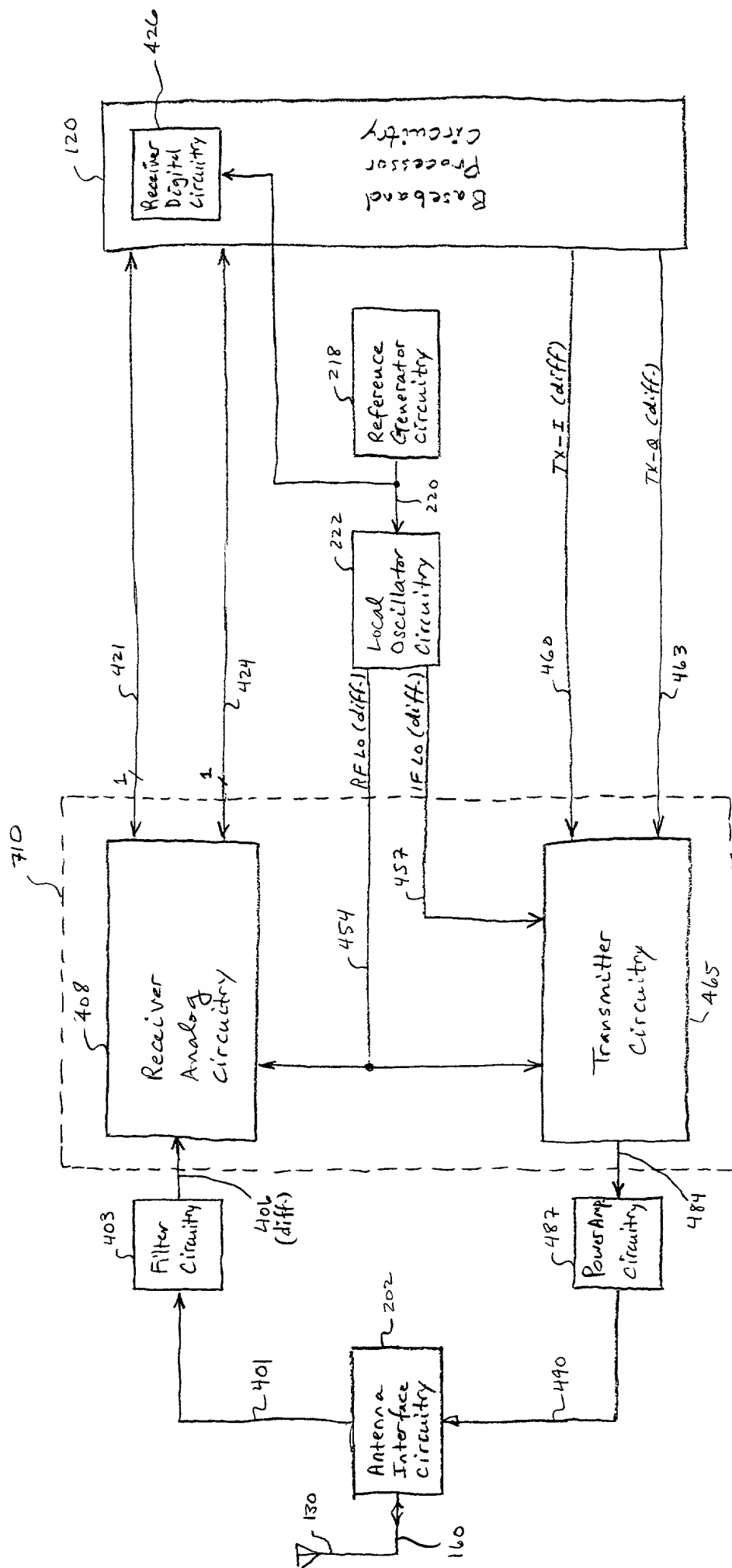


FIG. 7

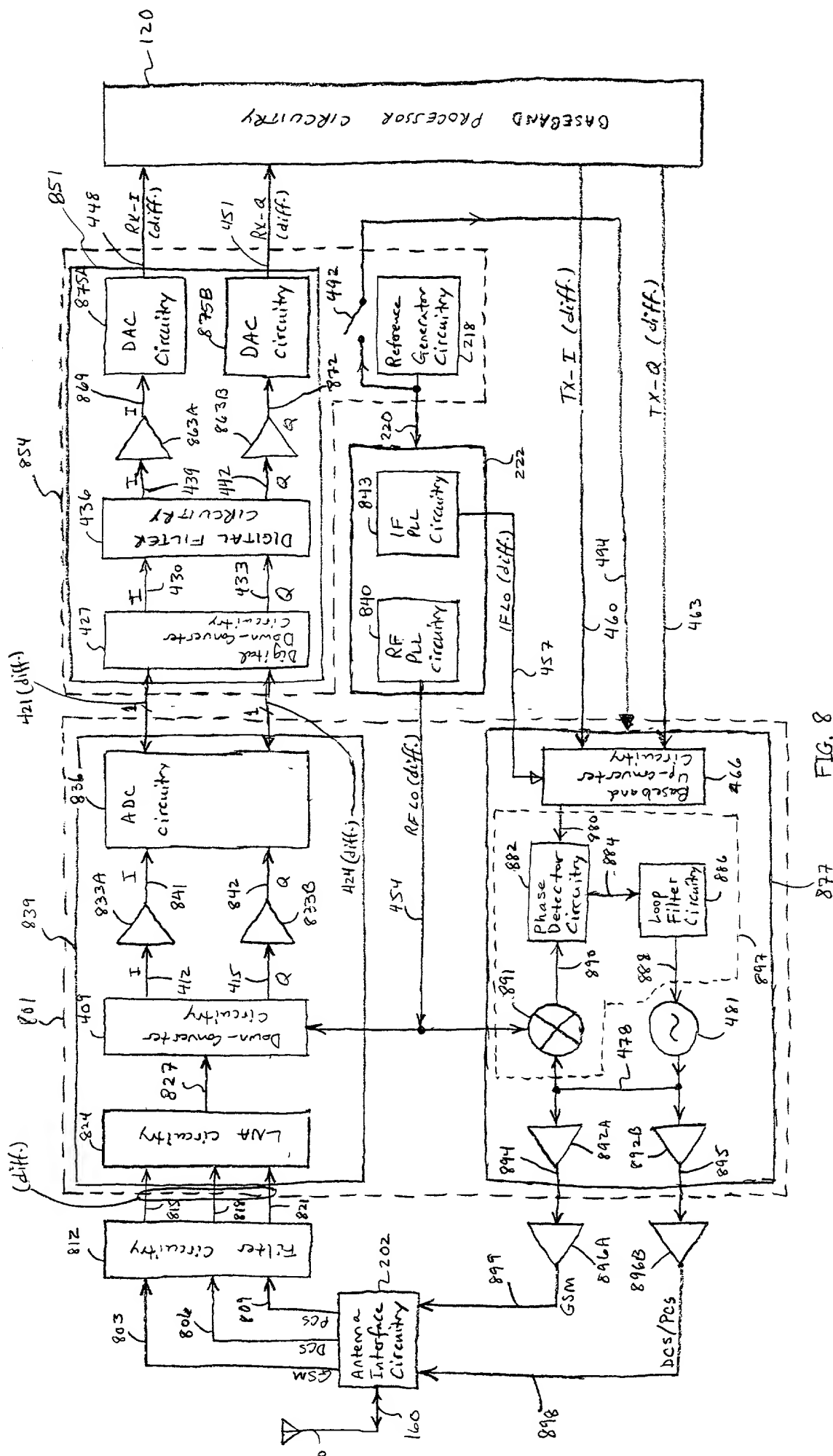


FIG. 8

FIG. 9A

900A

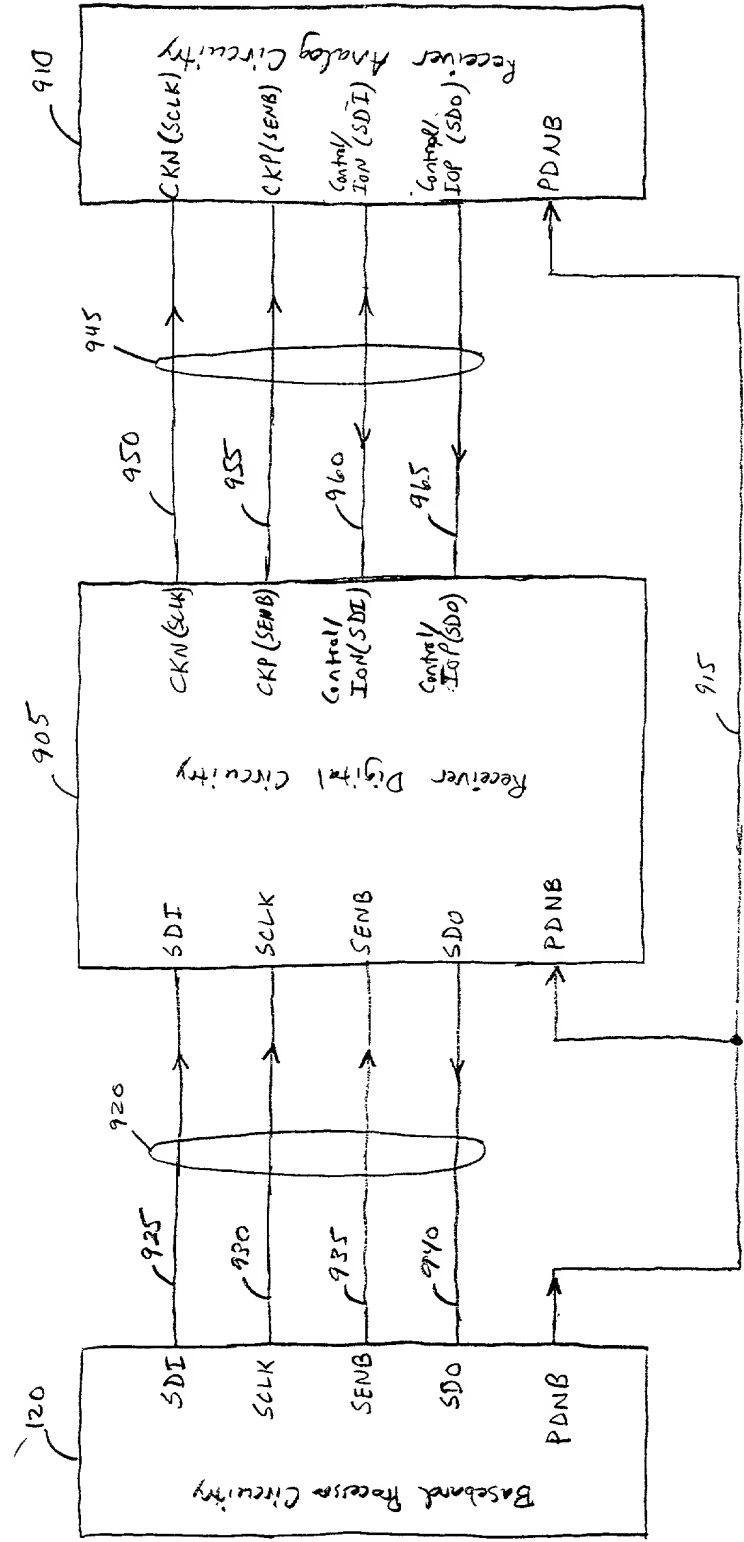


FIG. 9A

900B

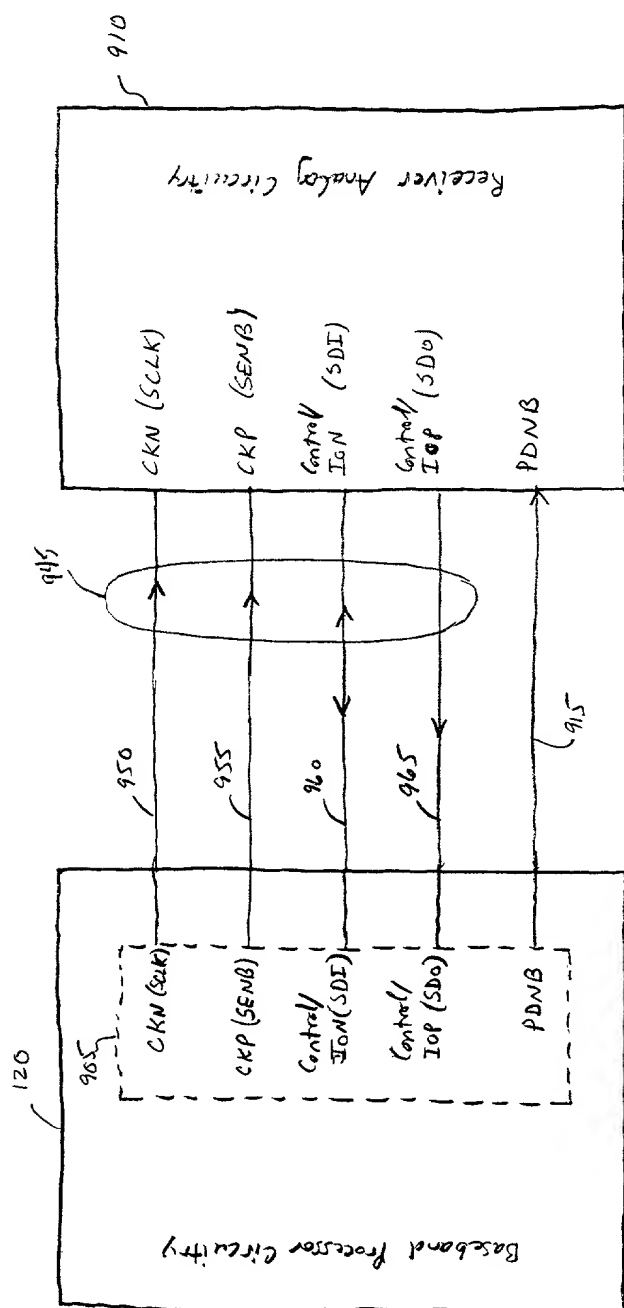


FIG. 9B

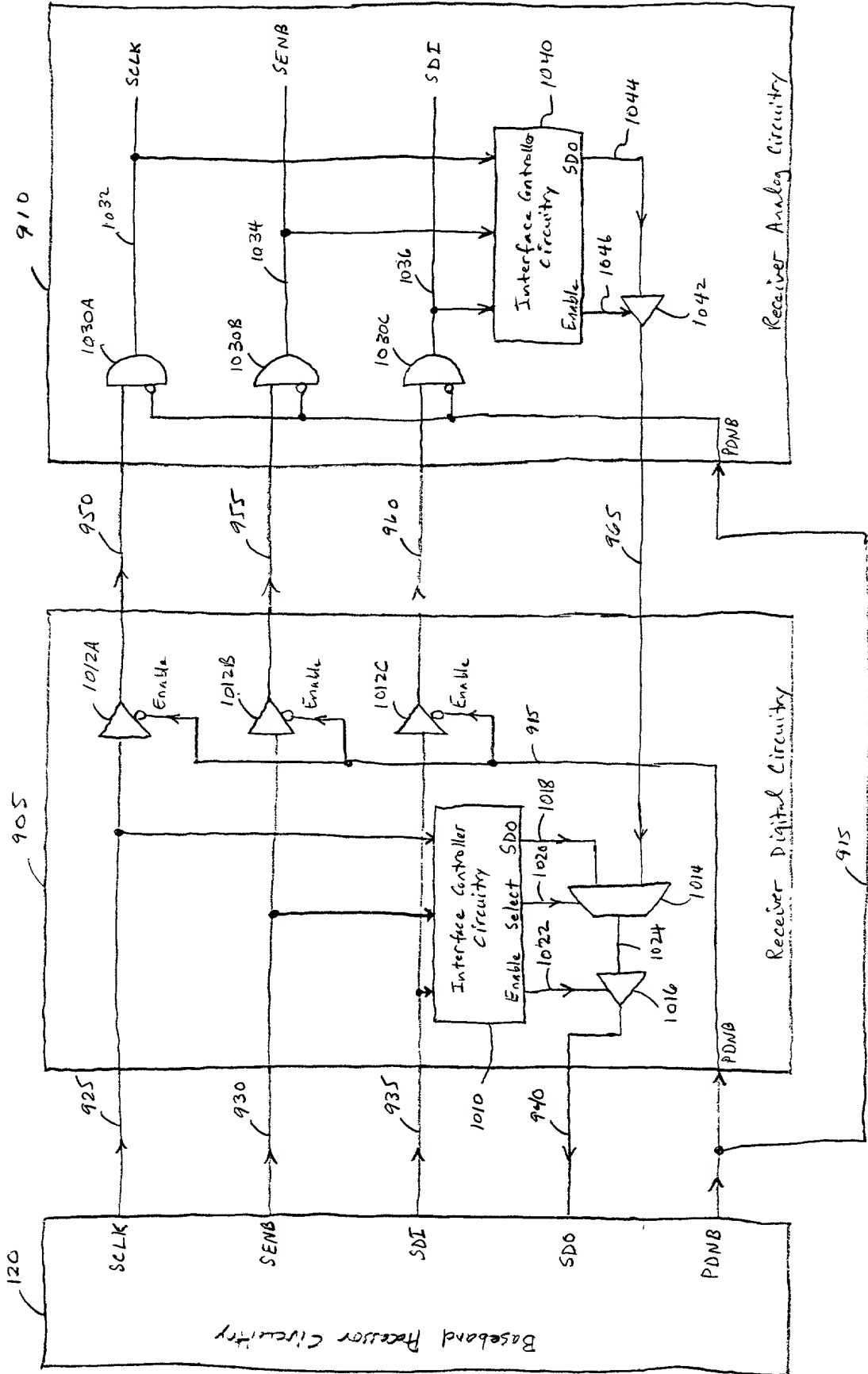


FIG. 10

1180A

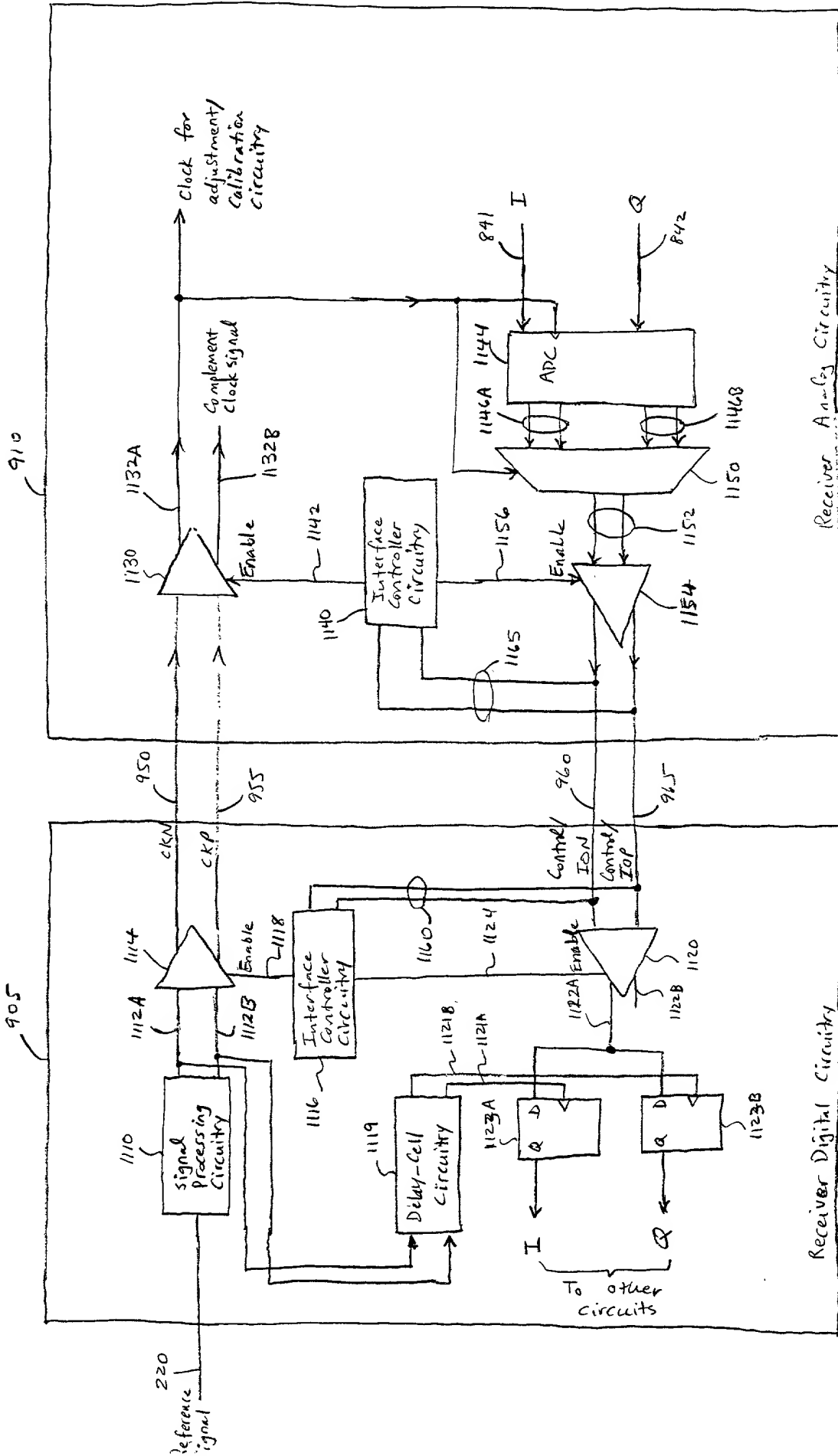


FIG. 11A

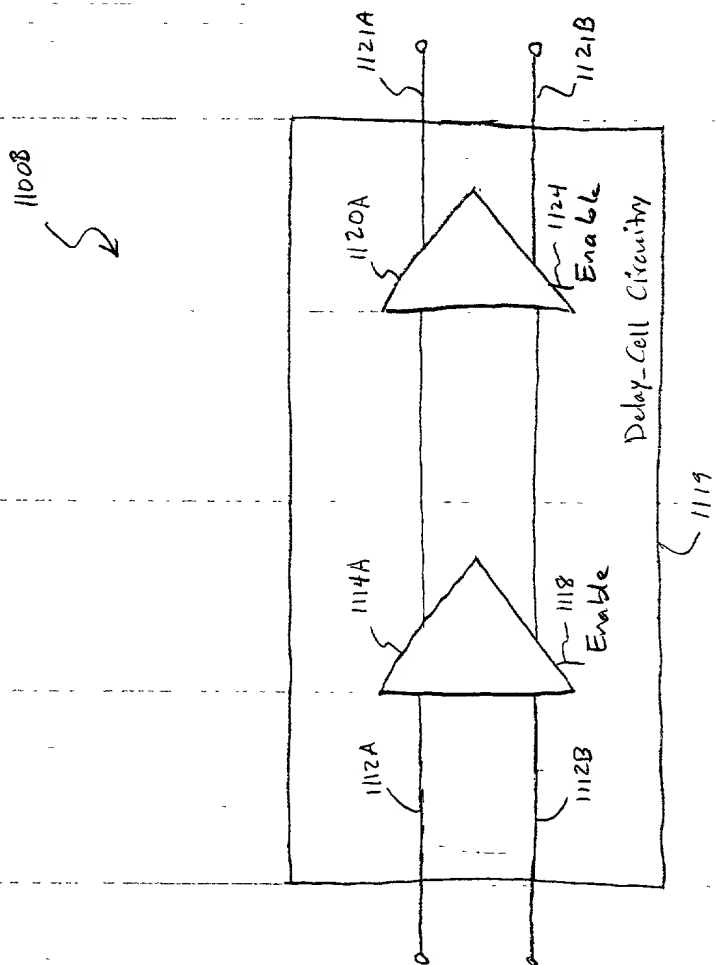


FIG. 11B



1200

1200

CLOCK SIGNAL

VDD

Enable

1203

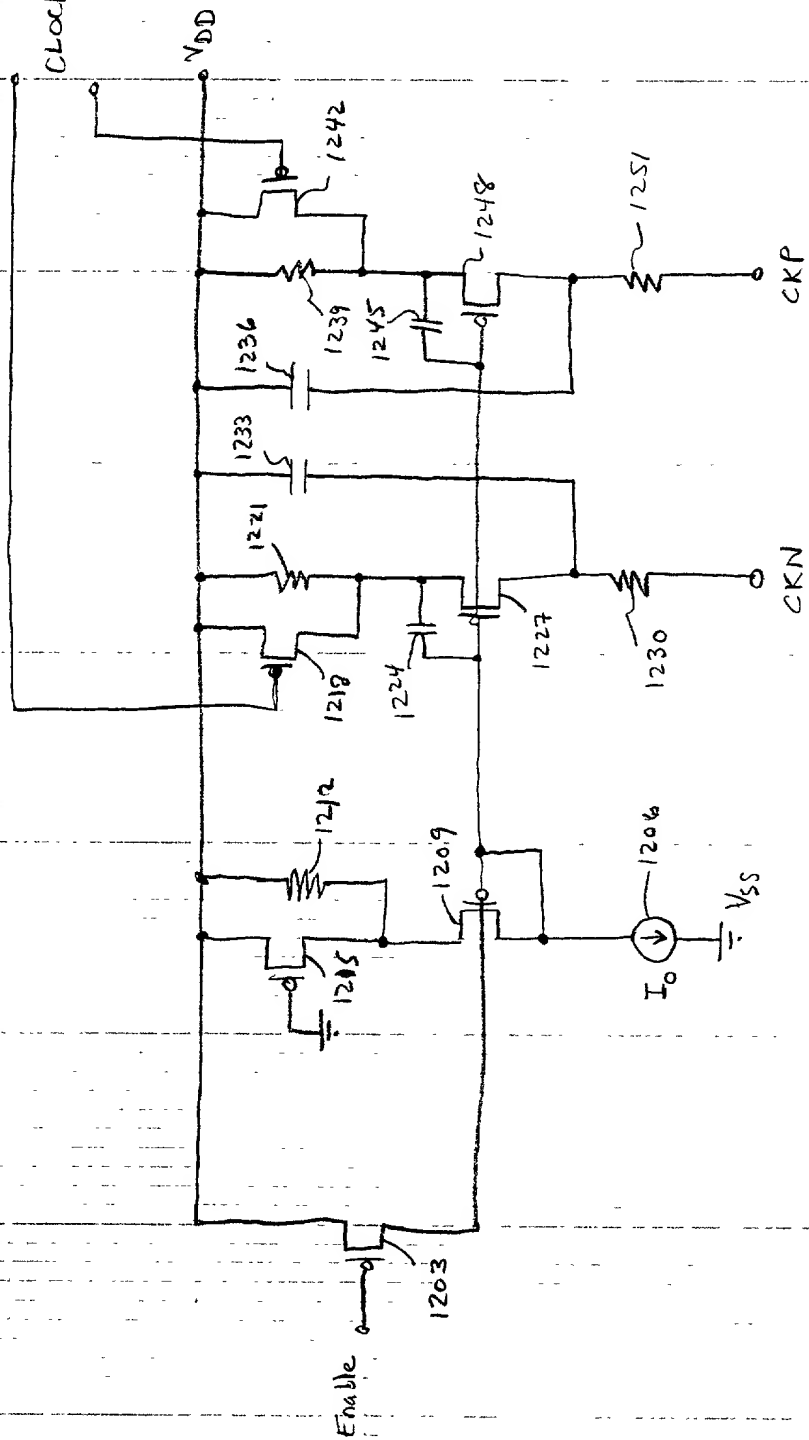
$I_o$

VSS

CKN

CKP

FIG. 12





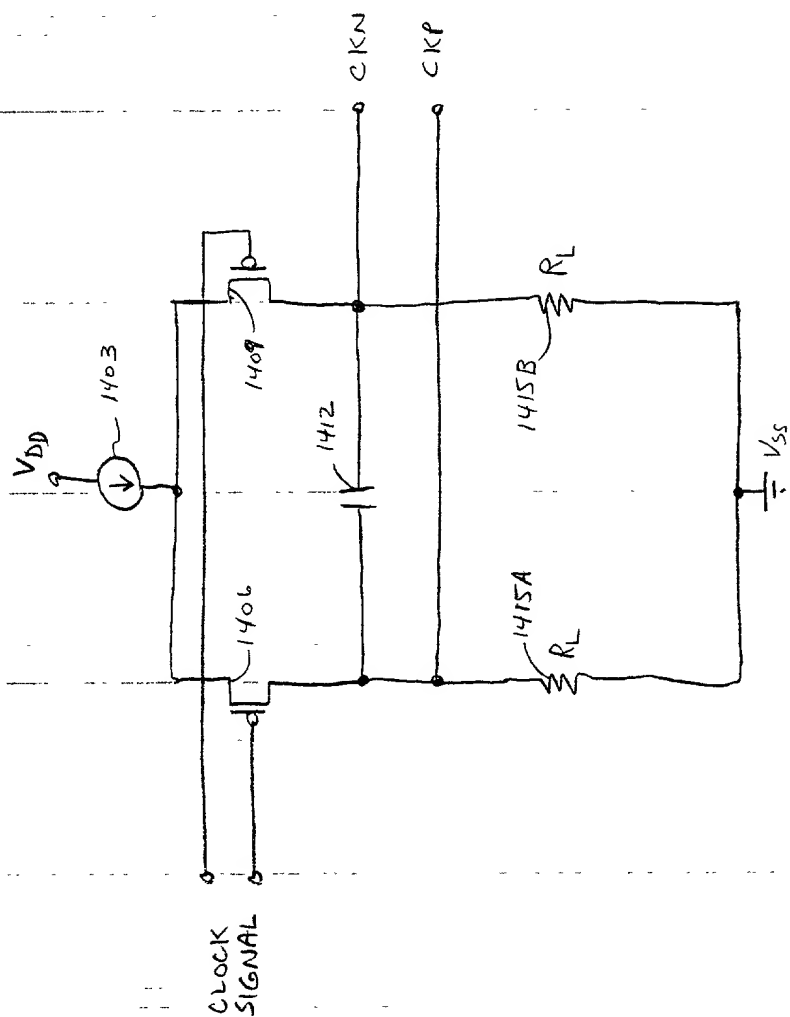


FIG. 14